**VLSI PROJECTS LIST(2019-20)**

1. Dual-Quality 4:2 Compressors For Utilizing In Dynamic Accuracy Configurable Multipliers.
2. Multipliers-Driven Perturbation Of Coefficients For Low-Power Operation In Reconfigurable Fir Filters.
3. Roba Multiplier: A Rounding-Based Approximate Multiplier For High-Speed Yet Energy-Efficient Digital Signal Processing.
4. Design Of Efficient BCD Adders In Quantum-Dot Cellular Automata.
5. Power Delay Product Optimized Hybrid Full Adder Circuits.
6. Analysis Of Vedic Multiplier Using Various Adder Topologies.
7. Design Of Low-Power High-Performance 2–4 And 4–16 Mixed-Logic Line Decoders.
8. Fm0 And Manchester Encoding Using Sols Technique With Clock Gating & Power Gating Methods.
9. Reconfigurable Delay Optimized Carry Select Adder VLSI Design For Convolutive Blind Source Separation.
10. Reconfigurable Constant Multiplication For Fpgas.
11. Design Of Power And Area Efficient Approximate Multipliers.
12. Multipliers-Driven Perturbation Of Coefficients For Low-Power Operation In Reconfigurable FIR Filters.
13. A Computationally Efficient Reconfigurable Constant Multiplication Architecture Based On CSD Decoded Vertical–Horizontal Common Sub-Expression Elimination Algorithm.
14. Design Of Low Power 8-Bit Carry Select Adder Using Adiabatic Logic.
15. Hardware Design Of An Energy-Efficient High-Throughput Median Filter.
16. VLSI Implementation Of 3D Integer DCT For Video Coding Standards.
17. Low-Cost High-Performance VLSI Architecture For Montgomery Modular Multiplication.
18. Pre-Encoded Multipliers Based On Non-Redundant Radix-4 Signed-Digit Encoding.
19. Delay Efficient Error Detection And Correction Of Parallel IIR Filters Using VLSI Algorithms.
20. Addition Of Miller And Inverted Manchester Encoding Technique To Dedicated Short Range Communication With Full Hardware Utilization.
21. Analysis And Design Of Low-Power Reversible Carry Select Adder Using D-Latch.
22. A Modified Partial Product Generator For Redundant Binary Multipliers.
23. An Efficient VLSI Architecture For Data Encryption Standard And Its FPGA Implementation.
24. A Normal I/O Order Radix-2 FFT Architecture To Process Twin Data Streams For MIMO.
25. Design Of Delay Efficient Modified 16 Bit Wallace Multiplier.
26. Low Power Area Efficient Alu With Low Power Full Adder.
27. A Cellular Network Architecture With Polynomial Weight Functions.
28. Carry Speculative Adder With Variable Latency For Low Power VLSI.
29. A New VLSI Algorithm For A High-Throughput Implementation Of Type IV DCT.
30. Design And Implementation Of 64 Bit Multiplier Using Vedic Algorithm.
31. VLSI Architecture For Delay Efficient 32-Bit Multiplier Using Vedic Mathematic Sutras.
32. Delay Efficient Error Detection And Correction Of Parallel IIR Filters Using VLSI Algorithm.
33. A Modified Partial Product Generator For Redundant Binary Multipliers.
34. Concept, Design, And Implementation Of Reconfigurable CORDIC.
35. Design Of Fast FIR Filter Using Compressor And Carry Select Adder.
36. Design And Optimization Of 16×16 Bit Multiplier Using Vedic Mathematics.
37. High Performance VLSI Architecture For 3-D Discrete Wavelet Transform.
38. Carry Speculative Adder With Variable Latency For Low Power VLSI.
39. Design Of High Speed Carry Select Adder Using Brent Kung Adder.
40. VLSI Implementation Of Boolean Algebra Based Cryptographic Algorithm.
41. Iterative Architecture AES For Secure VLSI Based System Design.
42. An Efficient VLSI Architecture For Discrete Hadamard Transform.
43. An Efficient VLSI Architecture For Data Encryption Standard And Its FPGA Implementation.
44. Low Power Array Multiplier Using Modified Full Adder.
45. A Single-Ended With Dynamic Feedback Control 8T Sub threshold SRAM Cell.
46. Low-Power Scan-Based Built-In Self-Test Based On Weighted Pseudorandom Test Pattern Generation And Reseeding.
47. Implementation Of Multiplier Architecture Using Efficient Carry Select Adders For Synthesizing FIR Filters.
48. Low-Power Parallel Chine Search Architecture Using A Two-Step Approach.
49. Memory-Reduced Turbo Decoding Architecture Using NII Metric Compression.
50. Input-Based Dynamic Reconfiguration Of Approximate Arithmetic Units For Video Encoding.
51. High-Speed And Energy-Efficient Carry Skip Adder Operating Under A Wide Range Of supply Voltage Levels.
52. A Comparative Study Of FIR Filters Using Vedic And Booths Algorithm.
53. Hybrid LUT/Multiplexer FPGA Logic Architectures.
54. VLSI Architecture For Delay Efficient 32-Bit Multiplier Using Vedic Mathematic Sutras.
55. Low-Power And Area-Efficient Shift Register Using Pulsed Latches.
56. Scan Test Bandwidth Management For Ultra large-Scale System-On-Chip Architectures.
57. Fault Tolerant Parallel Filters Based On Error Correction Codes.
58. Low-Complexity Tree Architecture For Finding The First Two Minima.
59. Design Of Area And Delay Efficient Vedic Multiplier Using Carry Select Adder.
60. VLSI Computational Architectures For The Arithmetic Cosine Transform.
61. Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic.
62. Fully Reused VLSI Architecture Of FM0/Manchester Encoding Using SOLS Technique For DSRC Applications.
63. A Novel Fault Detection And Correction Technique For Memory Applications.
64. An Efficient Binary Multiplier Design For High Speed Applications Using Karatsuba Algorithm And Urdhva- Tiryagbhyam Algorithm.
65. Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic.
66. A Generalized Algorithm And Reconfigurable Architecture For Efficient And Scalable Orthogonal Approximation Of DCT.
67. Optimized Designs Of Reversible Fault Tolerant BCD Adder And Fault Tolerant Reversible Carry Skip BCD Adder.
68. A Modified Partial Product Generator For Redundant Binary Multiplier.
69. Ocnoc: Efficient One-Cycle Router Implementation For 3D Mesh Network-On-Chip.
70. FPGA Implementation Of Efficient Vedic Multiplier.
71. An Optimized Modified Booth Recoder For Efficient Design Of The Add-Multiply Operator.
72. Fault Tolerant Parallel Ffts Using Error Correction Codes And Parseval Checks.
73. Multifunction Residue Architectures For Cryptography.
74. 1.An Efficient Design Of 16 Bit MAC Unit Using Vedic Mathematics.
75. A Further Optimized Mix Column Architecture Design For The Advanced Encryption Standard.
76. Approximate Reverse Carry Propagate Adder For Energy-Efficient DSP Applications.
77. Architecture Optimization And Performance Comparison Of Nonce-Misuse-Resistant Authenticated Encryption Algorithms.
78. Low Power High Accuracy Approximate Multiplier Using Approximate High Order Compressors.
79. TOSAM:Anenergy-Efficienttruncation-Androunding-Basedscalableapproximate Multiplier.
80. Efficient Modular Adder Designs Based On Thermometer & One-Hot Encoding.
81. 8.FPGA Based Implementation Of FIR Filter For FOFDM Waveform.
82. Design And Analysis Of Approximate Redundant Binary Multipliers.
83. Design Of Reversible Arithmetic Logic Unit With Built-In Testability.
84. A Combined Arithmetic-High-Level Synthesis Solution To Deploy Partial Carry-Save Radix-8 Booth Multipliers In Data path.
85. Ultra-Low-Voltage GDI-Based Hybrid Full Adder Design For Area And Energy-Efficient Computing Systems.
86. Low Power Approximate Unsigned Multipliers With Configurable Error Recovery.
87. A Two Speed Radix -4 Serial –Parallel Multiplier.
88. Performance Analysis Of Wallace Tree Multiplier With Kogge Stone Adder Using 15-4 Compressor.
89. Concurrent Error Detectable Carry Select Adder With Easy Testability.
90. Design And Analysis Of Majority Logic Based Approximate Adders And Multipliers.
91. Block-Based Carry Speculative Approximate Adder For Energy-Efficient Applications.