**DESIGN AND ANALYSIS OF MAJORITY LOGIC BASED APPROXIMATE ADDERS AND MULTIPLIERS**

**Abstract:**

As a new paradigm for nanoscale technologies, approximate computing deals with error tolerance in the computational process to improve performance and reduce power consumption. Majority logic (ML) is applicable to many emerging nanotechnologies; its basic building block (the 3-input majority voter, MV) has been extensively used for digital circuit design. In this paper, designs of approximate adders and multipliers based on ML are proposed; the proposed multipliers utilize approximate compressors and a reduction circuitry with so-called complement bits. An inﬂuence factor is deﬁned and analyzed to assess the importance of different complement bits depending on the size of the multiplier; a scheme for selection of the complement bits is also presented. The proposed designsareevaluatedusinghardwaremetrics(suchdelayandgatecomplexity)aswellaserrormetrics.ComparedwithotherML-based designs found in the technical literature, the proposed designs are found to offer superior performance. Case studies of error-resilient applications are also presented to show the validity of the proposed designs.

**Index Terms—**majority logic, approximate adder, approximate multiplier, complement bits, approximate compressor, image processing.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**