**CONCURRENT ERROR DETECTABLE CARRY SELECT ADDER WITH EASY TESTABILITY**

**Abstract:**

A concurrent error detectable adder with easy testability is proposed. The proposed adder is based on a multi-block carry select adder. Any erroneous output of the adder caused by a fault modeled as a single stuck-at fault can be detected by comparing the predicted parity of the sum with the parity of the sum, i.e., the XORed value of the sum bits, and comparing the duplicated carry outputs. The adder is also testable with only 10 input patterns under single stuck-at fault model. This property eases detection of a fault before the occurrence of a second fault. Both the concurrent error detectability to detect erroneous results and the easy testability to ﬁnd a fault during operation are important for realizing reliable systems. Both the concurrent error detectability and the easy testability of the proposed adder are proven. A 32-bit adder has been designed. Its hardware overhead is about 70%. Its concurrent error detectability and 100% test coverage through the 10 patterns has been conﬁrmed by fault simulation.

**Index Terms—**Concurrent error detection, carry select adder, design for testability.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**