**COMPUTER ARITHMETIC ARCHITECTURES WITH REDUNDANT NUMBER SYSTEMS**

**Abstract:**

Redundant arithmetic number systems are gain- ing popularity in computationally intensive environ- ments particularly because of the carry-free addi- tion/subtraction properties they possess. This prop- erty has enabled arithmetic operations such as addi- tion, multiplication, division, square root, etc., to be performed much faster than with conventional binary number systems. In this paper, some of the recent con- tributions to the area of design of redundant arithmetic based addition, multiplication, division, and square root algorithms and architectures are briefly discussed. Also, only the use of bit/digit-parallel implementation for architectures is discussed so that the enhancement in speed through the use of redundant arithmetic be- comes immediately apparent as opposed to the use of bit/digit-serial architectures, where the primary justi- fication for their use is to conserve area. A new radix 2 division algorithm using over-redundant radix 2 quo- tient digits and requiring a 2 digit quotient selection function is also presented.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**