**ULTRA-LOW-VOLTAGE GDI-BASED HYBRID FULL ADDER DESIGN FOR AREA AND ENERGY-EFFICIENT COMPUTING SYSTEMS**

**Abstract:**

In recent years, ultra-low-voltage (ULV) operation is gaining more importance for achieving minimum energy consumption. Full adder is the basic computational arithmetic block in many of the computing and signal/image processing applications. Here, a new hybrid 1-bit full adder circuit which employs both Gate Diffusion Input (GDI) logic and multi-threshold voltage (MVT) transistor logic is reported. The main objective of the proposed MVT-GDI-based hybrid full adder design is to provide minimum energy consumption with less area. The proposed hybrid design is simulated using standard 45 nm CMOS process technology at an ULV of 0.2 V. The post-layout simulation results have shown that the proposed design achieved significant improvements in comparison with the other reported designs by achieving >57%, 92% savings in the Energy and EDP, respectively, with only 14 transistors. Monte–Carlo simulations have also been performed and is found that the proposed design methodology yields full functionality and robustness against local and global process variations. Normalised energy metrics to 32 and 22 nm technologies shows that the proposed design achieves >57% energy savings in prior to the recent works.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**