**DESIGN OF REVERSIBLE ARITHMETIC LOGIC UNIT WITH BUILT-IN TESTABILITY**

**Abstract:**

Reversibility is one of the foundations for various emerging technologies like quantum ,DNA and optical computing. It may be used for designing ultra low power circuits, which will help to reduce the total energy consumption worldwide. Testing of these circuits has also been a major concern to validate their functionality. This Paper presents a novel design of Arithmetic Logic Unit (ALU) that can be scalable up to N number of bits. The design process utilizes the properties of Toffoli and Fredkin gates to make the circuit parity preserving which shows its in-built testability feature. Proposed architecture provides full coverage of single bit faults in the circuit. The design and implementation is performed over reversible circuit analyser for obtaining operating costs in terms of number of inputs, gate count, quantum cost, garbage outputs and ancilla inputs. Recently reported reversible ALU architectures are compared with proposed work on a single platform ,where we have achieved a reduction up to 61% in the gate cost.

**Index Terms**—Reversible Logic Circuits, ALU, DFT, Fault Detection.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**