**FM0 AND MANCHESTER ENCODING USING SOLS TECHNIQUE WITH CLOCK GATING & POWER GATING METHODS**

**Abstract:**

The benchmarks of Manchester codes and FM0 are prevails to dc-leveling, im-demonstrating territory, power and postponement. The coding-grouped qualities between the Manchester codes and FM0 truly confine likelihood which style a plot of completely reused VLSI for each. In this paper, the similitude situated rationale improvement (SOLS) methodology is relied upon to beat this limitation. The SOLS framework upgrades the hardware utilize rate from 57.14% to 100% for FM0 and Manchester encodings. The proposed framework utilized is power diminishment procedures i.e.; clock gating and control gating strategies. The clock gating is to lessen the dynamic power dissemination and clock signals. Control gating is to decrease static power dissemination. This paper not just adds independently to a completely reused VLSI framework and abatements region to 14.2%, delay had a fall by 33.3% and power diminishment to 67.3% utilizing these two techniques

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**