**AN OPTIMIZED MODIﬁED BOOTH RECODER FOR EFﬁCIENT DESIGN OF THE ADD-MULTIPLY OPERATOR**

**Abstract:**

Complex arithmetic operations are widely used in Digital Signal Processing (DSP)applications. In this work, we focus on optimizing the design of the fused Add-Multiply (FAM) operator for increasing performance. We investigate techniques to implement the direct recoding of the sum of two numbers in its Modiﬁed Booth (MB) form. We introduce a structured and efﬁcient recoding technique and explore three different schemes by incorporating them in FAM designs .Comparing them with the FAM designs which use existing recoding schemes, the proposed technique yields considerable reductions in terms of critical delay, hardware complexity and power consumption of the FAM unit.

**Index Terms**—Add-Multiply operation, arithmetic circuits, Modiﬁed Booth recoding, VLSI design.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**