**FPGA IMPLEMENTATION OF AN EFFICIENT VEDIC MULTIPLIER**

**Abstract:**

Multipliers are the most significant components in the design of many high performance FIR filters, image and digital signal processors in the upcoming digital world. Multipliers being the most area and power consuming elements of a design, area-efficient low-power multiplier architectures are in demand. In this paper, multiplier based on ancient Vedic mathematics technique has been proposed which employs full adders, compressors and other efficient components to achieve the desired parameters for the proposed design. Combining the Vedic Sutras - urdhva tiryagbhyam sutra and efficient compressors, a robust speed and area efficient multiplier architecture is achieved. The proposed multiplier is designed in VHDL and simulated using Xilinx and Modelsim softwares.

**Keywords**— Vedic mathematics, Xilinx, Compressor, Urdhva triyakbhyam sutra.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**