**DESIGN OF LOW-POWER HIGH-PERFORMANCE 2–4 AND 4–16 MIXED-LOGIC LINE DECODERS**

**Abstract:**

This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2–4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aimingonhighpower-delayperformance.Bothnormalandinverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4–16 decoders are designed by using mixed-logic 2–4 predecoders combined with standard CMOS postdecoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spicesimulationsat32nmshowsthattheproposedcircuitspresent a signiﬁcant improvement in power and delay, outperforming CMOS in almost all cases.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**