**OPTIMIZED DESIGNS OF REVERSIBLE FAULT TOLERANT BCD ADDER AND FAULT TOLERANT REVERSIBLE CARRY SKIP BCD ADDER**

**Abstract:**

In recent years, reversible logic has become one of the most important areas of researches because of its applications in several technologies; such as low-power CMOS, Nanocomputing and optical computing. In this paper, we have presented designs of a compact and efficient fault tolerant reversible Binary Coded Decimal (BCD) adder as well as a fault tolerant reversible Carry Skip BCD adder. We have proposed new reversible fault tolerant gates and heuristic algorithms to design compact BCD Adders. The proposed reversible fault tolerant BCD adder achieves the improvement as reducing cost of 23.07% on the number of gates, 52.67% on quantum cost, 31.03% on garbage outputs, 29.16% on the number of constant inputs and 23.07% on unit delay over the existing best one. Similarly, the proposed reversible fault tolerant carry skip BCD adder achieves the improvement as reducing cost of 34.72% on the number of gates, 43.24% on quantum cost, 37.5% on garbage outputs, 37.14% on the number of constant inputs and 34.72% on unit delay over the existing best one.

**Keywords—** Reversible, UFT, Overflow detection logic, Fault Tolerance and BAFTA etc

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**