**FLEXIBLE DSP ACCELERATOR ARCHITECTURE EXPLOITING CARRY-SAVE ARITHMETIC**

**Abstract:**

Hardware acceleration has been proved an extremelypromising implementation strategy for the digital signal processing (DSP)domain. Rather than adopting a monolithic application-specific integratedcircuit design approach, in this brief, we present a novel acceleratorarchitecture comprising flexible computational units that support theexecution of a large set of operation templates found in DSP kernels.We differentiate from previous works on flexible accelerators by enablingcomputations to be aggressively performed with carry-save (CS) formatteddata. Advanced arithmetic design concepts, i.e., recoding techniques,are utilized enabling CS optimizations to be performed in a larger scopethan in previous approaches.The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

**Enhancement of the project:**

Perform the other temple of the FCU

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**