**IMPLEMENTATION OF AN EFFICIENT FLOATING POINT MULTIPLIER USING KARATSUBA AND URDHVA-TIRYAGBHYAM ALGORITHM**

**Abstract:**

Floating point multiplication is a key Significance to Many modern applications such as image processing, signal processing etc. The performance of DSP systems usually decided with the performance of the multiplier because the multiplier is the slowest constituent in the system. As, the multiplication dominates the execution time of most of the DSP application, hence a high speed multiplier is much preferred. This paper proposes an effective scheme for floating point multiplication that offers a superior implementation in terms of delay and area. A group of Karatsuba and Urdhva-Tiryagbhyam algorithm is used to implement a binary multiplier for mantissa multiplication. The IEEE 754 format used for the representation of a floating point number. The algorithms are implemented with Verilog (HDL) and targeted on FPGA Vertex 5 board and for the simulation purpose Xilinx ISE simulator is used and a table of delay performance, device utilization is made.

**Keywords:** Floating point format., UrdhvaTiryagbhyam., Karatsuba, .Fpga, Vedic mathematics

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**