**VLSI COMPUTATIONAL ARCHITECTURES FOR THE ARITHMETIC COSINE TRANSFORM**

**Abstract:**

The Discrete Cosine Transform (DCT) method is a mostly used one in DSP applications. This paper presents low power Algorithmic Noise TolerACT (ACT) predicated Discrete Cosine Transform (DCT) architectures utilizing mertens calculation block (MCB) and Multiply and Accumulate (MAC) units. The ACT predicated DCT architecture utilizing MAC units is proposed for DCT implementation where the puissance consumption and area consumption are reduced over the ACT predicated DCT architecture utilizing (MCB). In this paper, the eight point DCT architectures are designed for both 8-bit and 12-bit and withal compared. The puissance consumption and area involution are reduced by minimizing number of arithmetic operations in MAC predicated DCT architecture. The Voltage OverScaling (VOS) method is utilized in ACT technique for low power dissipation. By utilizing Process, Voltage and Temperature (PVT) variations, the potency consumption can be reduced.

**Keywords:** ACT algorithm, Discrete Cosine Transform (DCT), Multiply And Accumulate(MAC), Matrix Factorization of ACT

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**