**ANALYSIS OF VEDIC MULTIPLIER USING VARIOUS ADDER TOPOLOGIES**

**Abstract:**

Vedic maths based multiplier is a novel and high speed multiplier. Adder is one of the main components used in this technique. Using fast adder will enhance the overall performance of the Vedic multiplier. In this work, comparative analysis is done using different adder architectures in Synopsis Design Compiler with different standard cell libraries at 32/28 nm. Various Adder topologies like Ripple Carry Adder (RCA), Carry Select Adder (CSA), Square Root Carry Select Adder (SQRT-CSA), Common Boolean Logic (CBL) and Binary to Excess one Converter (BEC) are used to compare area, delay and power. Designing is done for 8-bit, 16-bit, 32-bit and 64-bit Vedic multiplier using the above adders. It is found that 64-bit Vedic multiplier using SQRT-CSA adder is approximately 5% faster than RCA-CSA and BEC, 75% faster than CBL and RCA

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**