**DESIGN OF VEDIC MULTIPLIER USING SQRT CARRY SELECT ADDER (CSLA)**

**Abstract:**

Vedic multiplier is designed using area-efficient Carry Select Adder (CSLA). As the multiplication is the process of subsequent addition, adder is important block in implementation of multiplier. Digital adder has problem of carry propagation, thus carry select adder is used instead of simple Ripple Carry Adder (RCA). Carry select adder is known to be one of the fastest adder structures. Here Vedic multiplier is implemented instead of normal multipliers like add and shift multiplier, array multiplier etc. The goal is to design Vedic multiplier based on crosswise and vertical algorithms using area efficient Sqrt CSLA. Conventional CSLA designs like Binary to Excess one Converter (BEC) based CSLA and Modified CSLA (MCSLA) are compared with proposed CSLA design to prove its efficiency. It shows improved performance in terms of area. This renovated CSLA is used to design proposed Vedic multiplier. The proposed Sqrt CSLA based Vedic multiplier provides better results in power and speed of the digital circuits.

**Keywords:** Carry Select Adder, Ripple Carry Adder, and Binary to excess one Converter, Vedic Multiplier, Area-Efficient, and Delay

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**