**LOW-COMPLEXITY TREE ARCHITECTURE FOR FINDING THE FIRST TWO MINIMA**

**Abstract:**

This brief presents an area-efﬁcient tree architecture for ﬁnding the ﬁrst two minima as well as the index of the ﬁrst minimum, which is essential in the design of a low-density paritycheck decoder based on the min–sum algorithm. The proposed architecture reduces the number of comparators by reusing the intermediate comparison results computed for the ﬁrst minimum in order to collect the candidates of the second minimum. As a result, the proposed tree architecture improves the area–time complexity remarkably.

**Index Terms**—Area-efﬁcient design, digital integrated circuits, low-density parity-check (LDPC) codes, minimum value generation, tree structure

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**