**FAULT TOLERANT PARALLEL FILTERS BASED ON ERROR CORRECTION CODE**

**Abstract:**

Digital filters are widely used in signal processing and communication systems. In some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. Next many techniques that exploit the filters’ structure and properties to achieve fault tolerance have been proposed. As technology scales, it enables more complex systems that incorporate many filters. In those complex systems, it is common that some of the filters operate in parallel, for example, by applying the same filter to different input signals. Recently, a simple technique that exploits the presence of parallel filters to achieve fault tolerance has been presented. In this brief, that idea is generalized to show that parallel filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC This new scheme allows more efficient protection when the number of parallel filters is large. The proposed scheme coded in VHDL in Xilinx 12.2 and simulated using Modelsim10.1 and implemented on altera Cyclone IV FPGA.

**Keywords**: Error Correction Codes, Digital Filter, FPGA

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**