**DESIGN AND IMPLEMENTATION OF HYBRID LUT/MULTIPLEXER FPGA LOGIC ARCHITECTURES**

**Abstract:**

Hybrid configurable logic block architectures for field-programmable gate arrays that contain a mixture of lookup tables and hardened multiplexers are evaluated toward the goal of higher logic density and area reduction. Multiple hybrid configurable logic block architectures, both non factorable and factorable with varying MUX:LUT logic element ratios are evaluated across two benchmark suites (VTR and CHStone) using a custom tool flow consisting of LegUp-HLS, Odin-II front-end synthesis, ABC logic synthesis and technology mapping, and VPR for packing, placement, routing, and architecture exploration. VPR is used to model the new hybrid configurable logic block and verify post place and route implementation.. In this paper experimentally, we show that for non fractur able architectures, without any mapper optimizations, we naturally save up to∼8% area post place and route. For factorable architectures, experiments show that only marginal gains are seen after place-and-route up to∼2%. For both non factorable and factorable architectures, we see minimal impact on timing performance for the architectures with best area-efficiency.

Keywords— FPGA, Multiplexer logic element, Complex logic block, mapping technologies

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**