**INPUT-BASED DYNAMIC RECONFIGURATION OF VIDEO**

**ENCODING BY APPROXIMATE ARITHMETIC UNITS**

**Abstract:**

Image and video compression algorithms, such as JPEG, MPEG, and so on, are particularly attractive candidates for approximate computing which can be exploited to realize highly power-efficient implementations of these algorithms. However, existing approximate architectures typically fix the level of hardware approximation statically and are not adaptive to input data. For example, if a fixed approximate hardware configuration is used for an MPEG encoder the output quality varies greatly for different input videos. Architecture for MPEG encoders that optimizes power consumption with the goal of maintaining a particular Peak Signal-to-Noise Ratio (PSNR) threshold for any video. Toward this end, we design reconfigurable adder/sub tractor blocks (RABs), which have the ability to modulate their degree of approximation, and subsequently integrate these blocks in the motion estimation and discrete cosine transform modules of the MPEG encoder. We propose two heuristics for automatically tuning the approximation degree of the RABs in these two modules during runtime based on the Characteristics of each individual video. Note that although the proposed reconfigurable approximate architecture is presented for the specific case of an MPEG encoder, it can be easily extended to other DSP applications.

**Index Terms**: Approximate circuits, approximate, computing, low power design, quality configurable

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**