**POWER DELAY PRODUCT OPTIMIZED HYBRID FULL ADDER CIRCUITS**

**Abstract:**

Data processing performed by adder circuits need to achieve low delay and low power at the same time while maintaining low cost, due to the steep growth in mobile computation devices. Recently proposed 1-bit full adder design that hybridizes transmission gates (TG) and standard CMOS offers significant PDP improvement. Two full adder implementations are presented in this paper which further optimizes the previously presented circuits: First (CKT1) deploys GDI-cell based XNOR module to decrease PDP, while the second circuit (CKT2) reduces the worst case delay with equivalent PDP. Simulation results indicate the proposed CKT1 has 4.8% and 2.5% reduced PDP for realistic cascade and FO4 loads respectively, with 16% improved cost compared to literature. CKT2 maintains comparable PDP with 11.3% and 2% improved delay for realistic cascade and FO4 loads respectively

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**