**MEMORY-REDUCED TURBO DECODING ARCHITECTURE USING NII METRIC COMPRESSION**

**Abstract:**

 This paper proposes a new compression technique of next-iteration initialization (NII) metrics for relaxing the storage demands of turbo decoders. The proposed scheme stores only the range of state metrics as well as two indexes of the maximum and minimum values, while the previous compression methods have to store all the state metrics for initializing the following iteration. We also present a hardware-friendly recovery strategy, which can be implemented by simple multiplexing networks. Compared to the previous work, as a result, the proposed compression method reduces the required storage bits by 30%, while providing the acceptable error-correcting performance in practice.

**Index Terms—**Channel codes, communication systems, error- correction codes, memory compression, VLSI designs.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**