**LOW-POWER PARALLEL CHIEN SEARCH ARCHITECTURE USING A TWO-STEP APPROACH**

**Abstract:**

This brief proposes a new power-efﬁcient Chien search (CS) architecture for parallel Bose–Chaudhuri–Hocquenghem (BCH) codes. For syndrome-based decoding, the CS plays a signiﬁcant role in ﬁnding error locations, but exhaustive computation in cursa huge waste of power consumption. In the proposed architecture, the searching process is decomposed into two steps based on the binary matrix representation. Unlike the ﬁrst step accessed every cycle, the second step is activated only when the ﬁrst step is successful, resulting in remarkable power saving. Furthermore, an efﬁcient architecture is presented to avoid the delay increase in critical paths caused by the two-step approach. Experimental results show that the proposed two-step architecture for the BCH(8752, 8192, 40) code saves power consumption by up to 50% compared with the conventional architecture.

Index Terms—Bose–Chaudhuri–Hocquenghem (BCH) codes, Chien search (CS), low power, two-step approach.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**