**IMPLEMENTATION OF MULTIPLIER ARCHITECTURE USING EFFICIENT CARRY SELECT ADDERS FOR SYNTHESIZING FIR FILTERS**

**Abstract:**

This paper proposes design of an efficient constant multiplier architecture using carry select adders. The algorithms proposed earlier to implement this MCM for an efficient FIR filter design can be classified in two main groups graph based algorithms and common subexpression elimination algorithms (CSE). CSE algorithm uses binary representation of coefficients for the implementation of higher order FIR filter with a fewer variety of adders than Canonic Signed Digit (CSD)-based CSE methods. According to the VHBCSE Algorithm, initially 2-bit binary common sub-expression elimination algorithm has been applied vertically across adjacent coefficients on the 2-D space of the coefficient matrix followed by applying 4-bit and 8-bit BCSE algorithm horizontally within each coefficient. Thus there is reduced power consumption by minimum switching activity along with an improvement in the area and delay. The partial products generated by VHBCSE methodology and controlled additions are used by any efficient carry select adder(CSLA) to produce output efficiently instead of earlier ripple carry adderto reduce area and delay.

**Keywords** — CSLA;VHBCSE;CSEalgorithm;FIR filter;MCM

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**