**AN EFﬁCIENT VLSI ARCHITECTURE FOR DISCRETE HADAMARD TRANSFORM**

**Abstract:**

This paper proposes an efﬁcient VLSI architecture for discrete Hadamard transform, which is used in real time digital signal processing applications like image coding ,MPEG, and CDMA etc. The proposed N-point Hadamard transform architecture consists of signed carry save adder tree. So the depth of the architecture falls within the bounds of O(log2 N). Thesameproposedarchitectureisimplementedfor2D-discrete Hadamard transform, where the hardware utilization is full. In other words, row/column processing of 2D-transform is carried with same 1D-hardware. The performance results show that the proposed architecture gives better performance compared with existing architectures using 45 nm CMOS TSMC library. The proposed 8-point 1D-DHT achieves an improvement of 55.14% and 42.07% in worst path delay over conventional and linear systolic array based 1D-DHT architectures respectively. Similarly proposed 8×8-point 2D-DHT achieves an improvement of 50.7%, 21.7%, and 51.1% in worst path delay over conventional, linear systolic array, and distributed arithmetic based 2D-DHT architectures respectively.

**Keywords**-Distributed arithmetic; DSP processor; Hadamard Transform

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**