**ITERATIVE ARCHITECTURE AES FOR SECURE VLSI BASED SYSTEM DESIGN**

**Abstract:**

In this digital age of communication, private and confidential data is exchanged over internet and stored in digital mediums. This data is constantly under increasing threat. Encryption is one of the techniques to protect sensitive data. AES is considered to be one of most capable encryption algorithm in cryptography. AES can be implemented in hardware or software. Hardware implementation would be faster and secure as compared to software implementation. This paper explains iterative architecture implementation of AES using VHDL

**Keywords**—Encryption; AES; Crptography; Iterative; VHDL

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**