**HIGH SPEED VLSI ARCHITECTURE FOR 3-D DISCRETE WAVELET TRANSFORM**

**Abstract:**

This paper presents a memory efﬁcient, high throughput parallel lifting based running three dimensional discrete wavelet transform (3-D DWT) architecture. 3-D DWT is constructed by combining the two spatial and four temporal processors. Spatial processor (SP) apply the two dimensional DWT on a frame, using lifting based 9/7 ﬁlter bank through the row rocessor (RP) in row direction and then apply in the colum direction through column processor (CP). To reduce the temporal memory and the latency, the temporal processor (TP) has been designed with lifting based 1-DHaar waveletﬁlter. The proposed architecture replaced the multiplications by pipeline shift-addoperations to reduce the CPD. Two spatial processors works simultaneously on two adjacent frames and provide 2-D DWT coefﬁcients as inputs to the temporal processors. TPs apply the one dimensional DWT in temporal direction and provide eight 3-D DWT coefﬁcients per clock (throughput). Higher throughput reduces the computing cycles per frame and enable the lower power consumption. Implementation results shows that the proposed architecture has the advantage in reduced memory, low power consumption, low latency, and high throughput over the existing designs. The RTL of the proposed architecture is described using verilog and synthesized using 90-nm technology CMOS standard cell library and results show that it consumes 43.42 mW power and occupies an area equivalent to 231.45 K equivalent gate at frequency of 200 MHz. The proposed architecture has also been synthesised for the Xilinx zynq 7020 series ﬁeld programmable gate array (FPGA).

**Index Terms** : discrete wavelet transform, 3-D DWT, lifting based DWT, VLSI Architecture, ﬂipping structure, strip-based scanning.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**