**DESIGN AND OPTIMIZATION OF 16×16 BIT MULTIPLIER USING VEDIC MATHEMATICS**

**Abstract:**

Multiplication is basic function in arithmetic operations. Multiplication based operations such as multiply and Accumulate unit (MAC), convolution, Fast Fourier Transform (FFT), filtering are widely used in signal processing applications. As, multiplication dominates the execution time of DSP systems, there is need to develop high speed multipliers. Ancient Vedic mathematics facilitates the solution to some extent. In this paper, concept of Urdhwa-Tiryagbhyam is used i.e., vertically and crosswise multiplication to implement 16×16 Bit Vedic multiplier and optimization is achieved by using carry save adders. Comparing with previous architectures, proposed architecture achieves 33.26% reduction in combinational path delay. The Vedic multiplier proposed is implemented in VHDL whereas synthesized and simulated using Xilinx ISE Design Suite 14.5.

**Keywords—** Vedic Mathematics, MAC, Carry Save Adders, Urdhwa-Tiryagbhyam.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**