**VLSI ARCHITECTURE FOR DELAY EFFICIENT 32-BIT MULTIPLIER USING VEDIC MATHEMATIC SUTRAS**

**Abstract:**

This paper presents the VLSI Architecture for High-Speed 32-bit Multiplier using Vedic Mathematic sutras. Two sutras among 16 sutras of Vedic Mathematics can be applied for multiplication. Nikhilam Sutra and UrdhvaTiryagbhyam Sutra are used to implement Vedic Multipliers. In this paper, VLSI architecture for both sutras is implemented and synthesized in Xilinx software. The delay and memory for multiplier using Urdhva-Tiryagbhyam sutra are less when compared to multiplier using Nikhilam sutra. Further, the structure of Vedic Multiplier is modified by using Binary to excess-1 code converter so as to obtain less delay for the multiplier. By replacing normal adders with Binary to excess-1 code converter in multipliers we can achieve reduction in delay.

**Keywords—** Vedic mathematics, Vedic multiplier, UrdhvaTiryagbhyam, Nikhilam Navatashcaramam Dashatah, Ripple Carry Adder (RCA), Carry Select Adder (CSLA), Binary to Excess-1 Code Converter (BEC-1).

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**