**PRE-ENCODED MULTIPLIERS BASED ON NON-REDUNDANT RADIX-4 SIGNED-DIGIT ENCODING**

**Abstract:**

In this paper, we introduce an architecture of pre-encoded multipliers for Digital Signal Processing applications based on off-line encoding of coefﬁcients. To this extend, the Non-Redundant radix-4 Signed-Digit (NR4SD) encoding technique, which uses the digit values {−1,0,+1,+2} or {−2,−1,0,+1}, is proposed leading to a multiplier design with less complex partial products implementation. Extensive experimental analysis veriﬁes that the proposed pre-encoded NR4SD multipliers, including the coefﬁcients memory, are more area and power efﬁcient than the conventional Modiﬁed Booth scheme.

**Index Terms—**Multiplying circuits, Modiﬁed Booth encoding, Pre-Encoded multipliers, VLSI implementation

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**