**HARDWARE DESIGN OF AN ENERGY-EFFICIENT HIGHTHROUGHPUT MEDIAN FILTER**

**Abstract:**

This paper presents a hardware design for an energyefficient, high-speed, one-dimensional median filter. Existing architectures focus on operating speeds, thus resulting in redundant power dissipation. This paper presents an algorithm and mathematical model for controlling the clock signals attached to circuit by analyzing the behavior of the filter, which immobilizes the data in registers and reduces not only signal transitions but also switching activities, thereby reducing the total dynamic power consumption. Furthermore, the proposed architecture provides high-speed computation. A median result can be produced in each clock cycle, and the maximum operating frequency performance is nearly independent of the filter size. The proposed architecture uses 90-nm process technology and experimental results show that the proposed method is more energy efficient than existing designs. The power consumption is reduced by 25% on average.

**Index Terms**—Low-Power, hardware, median filter, VLSI

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**