**DESIGN OF POWER EFFICIENT 8-BIT CARRY SELECT ADDER USING CEPAL**

**Abstract:**

This paper presents the design of low power 8-bit Carry Select Adder (CSLA) using Complementary energy Path Adiabatic Logic (CEPAL) . In all the arithmetic and DSP applications adders are the most essential blocks, especially in design of DSP hardware modules low power adders plays major role, As in FFT / DFT computations number adders and its power consumption will shows effect on overall power consumption of design. In this paper by considering power consumption as the major aspect, designed an 8-bit CEPAL carry select adder, this CEPAL Energy recovery circuits based on the adiabatic logic principle is a promising approach among other conventional approaches.The simulation of proposed design is carried out using Cadence 180nM CMOS technology with sinusoidal power supply at frequency of 1GHZ and compared it with the existing techologies.

**Keywords:** carry select adder, Full adder, CMOS Digital circuit design, Low-Power VLSI.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**