**A COMPUTATIONALLY EFﬁCIENT RECONﬁGURABLE CONSTANT MULTIPLICATION ARCHITECTURE BASED ON CSD DECODED VERTICAL–HORIZONTAL COMMON SUB-EXPRESSION ELIMINATION ALGORITHM**

**Abstract:**

 This paper introduces a computationally efﬁcient hardware architecture for reconﬁgurable multiple constant multiplication block, which functions according to the canonical signed digit (CSD)-based vertical and horizontal common subexpression elimination (VHCSE) algorithm. In the proposed architecture, the CSD decoded coefﬁcient along with 4-b common sub-expressions (CSs) in the vertical direction and 4- and 8-b CSs in the horizontal direction reduces the required number of full adder cells and the adder depths. This technique helps in reducing area consumption by decreasing the number of coefﬁcient multiplier adders by 59% than that of the binary VHCSE (VHBCSE) algorithm. This technique helps in reducing the average switching activity of the adder blocks used in each coefﬁcient multiplier block by 26.1%, 25.6%, and 21.3%, while compared with those of the 2- and 3-b binary CS elimination (BCSE) and VHBCSE algorithms, respectively. For different orders of ﬁlter, the proposed one delivers 57.5% and 61.9% improvement in area-power product (APP) on an average compared with the VHBCSE and mixed integer programming algorithms, respectively. Experimental results of differently speciﬁed ﬁnite impulse response (FIR) ﬁlters ranging from 10 to 100 taps and the coefﬁcients of 8, 12, and 16 b show the improvements of 42.8%, 53.6%, and 37%, respectively, in the average gate count and 51.8%, 43.5%, and 36.7% less propagation delay than those of earlier canonical double-based number representation method. Moreover, in the metric made of APP divided by throughput, the proposed technique experiences 63.7% improvement on an average over that of faithfully rounded truncated multiple constant multiplication/accumulation technique of designing constant multiplier and demonstrates its suitability for implementing efﬁcient reconﬁgurable FIR ﬁlter.

 **Index Terms**—Reconﬁgurable ﬁnite impulse response (FIR) ﬁlter, CSD based CSE algorithm, optimization technique, efﬁcient MCM, SDR system.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**