**RECONﬁGURABLE CONSTANT MULTIPLICATION FOR FPGAS**

**Abstract:**

This work introduces a new heuristic to generate pipelined run-time reconﬁgurable constant multipliers for FPGAs. It produces results close to the optimum. It is based on an optimal algorithm which fuses already optimized pipelined constant multipliers generated by an existing heuristic called RPAG. Switching between different single or multiple constant outputs is realized by the insertion of multiplexers. The heuristic searches for a solution that results in minimal multiplexer overhead. Using the proposed heuristic reduces the run-time of the fusion process, which raises the usability and application domain of the proposed method of run-time reconﬁguration. An extensive evaluation of the proposed method conﬁrmes a 9-26% FPGA resource reduction on average compared to previous work. For reconﬁgurable multiple constant multiplication, resource savings of up to 75% can be shown compared to a standard generic LUT multiplier. Two low level optimizations are presented, which further reduce resource consumption and are included into an automatic VHDL code generation based on the FloPoCo library.

**TOOLS:**

1. **XilinxISE 14.7**

**LANGUAGE:**

1. **VerilogHDL**